Source Second-Harmonic Control for High Efficiency Power Amplifiers

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***Abstract*—A novel technology that drastically improves output power and efficiency of amplifiers has been developed, where source and load second-harmonic impedances, as well as the fundamental impedances, are optimally terminated in the input and output matching circuits. A record high 74% power-added efficiency (PAE) with 31.4 dBm (1.4 W) output power at a frequency of 930 MHz has been achieved as a single-stage saturated amplifier using an ion-implanted GaAs MESFET under the low supply voltage of 3.5 V. As a single-stage linear amplifier, an excellent PAE of 59% with 31.5 dBm output power has been realized at V_d = 4.7 V and f = 948 MHz. Saturated and linear two-stage power modules operating at 900 MHz band with 31 dBm (1.25 W) output power have been demonstrated for analog and digital cellular applications respectively, the volume of which is as small as 0.4 cc. The saturated power module has achieved a PAE of 66% at V_d = 3.5 V, and the linear one has realized a PAE of 50% at V_d = 4.7 V.**

I. Introduction

ADVANCED HIGH PERFORMANCE hand-held phones require high efficiency power amplifiers with a low supply voltage [1], [2]. Since the power amplifiers are the highest power consumption components in portable equipment, the efficiency is directly related to the limit on talk time or battery life. Recently, digital mobile communication systems using digital modulation signal have been growing rapidly to provide large subscriber capacities and a variety of communication services. In these systems, high efficiency linear amplifiers [3]–[5] are required instead of saturated amplifiers.

In order to obtain high efficiency, many different types of power amplifiers such as Class F and tuned Class-B have been reported [6]–[10]. In these amplifiers, load impedances for the fundamental and harmonics are optimized so as to control voltage/current waveforms applied at the output terminal of an active device. By optimally terminating the harmonics up to the second harmonic, the theoretical maximum drain efficiency is reported to be 86% [8]. In another approach, a high efficiency amplifier has been realized by inputting a quasisquare voltage wave into the FET gate [11]. However, it is difficult to apply this technology to small sized power amplifiers because the quasisquare voltage wave has to be synthesized outside the amplifier.

We have found that a sinusoidal voltage wave inputted into a FET gate is transformed to a quasisquare wave by optimally terminating source second-harmonic impedance (Z_{S2}) [12]. Fig. 1 shows a circuit diagram of a developed single-stage amplifier, where both Z_{S2} and load second-harmonic impedance (Z_{L2}) can be optimally terminated with an approximate short circuit. In this paper, we describe the effects of tuning source second-harmonic impedance on output power and efficiency of GaAs MESFET's. The gate voltage and current waveforms analyzed by harmonic balance simulation are discussed. Power performance of a single-stage saturated amplifier and a two-stage saturated power module is presented in Section II. High efficiency operation of a single-stage linear amplifier and a two-stage linear power module is described in Section III.

II. Saturated Amplifier

A. Single-Stage Amplifier

A GaAs MESFET with a total gate width (W_g) of 12 mm was fabricated by an ion-implantation technology. By optimizing the device dimension and the fabrication process, low knee voltage (V_k) of I–V characteristics and high gate-to-drain breakdown voltage ($\mathrm{BV_{gd}}$) were attained [13]. The gate-source spacing (L_{gs}), the gate length (L_g), and the gate-drain spacing (L_{gd}) were 0.5, 0.6, and 1.0 μm respectively. An active channel was formed by Si ion-implantation at 80 KeV with a dose of 3.9×10^{12} cm^{-2}. The gate metal was Al/Ti, and the gate region was slightly recessed. The FET had V_k of 1.2 V, and had $\mathrm{BV_{gd}}$ of more than 20 V at a gate current density of 1 mA/mm. The saturation drain current at $V_g = 0$ V (I_{dss}) and pinch-off voltage were 3.0 A and −2.8 V, respectively. This FET was assembled in a metal-based package.

In order to investigate the power performance of the FET (W_g = 12 mm), an evaluation board was designed, the circuit diagram of which is shown in Fig. 1. Experimental procedures are described in the following. Source and load fundamental impedances (Z_{S1}, Z_{L1}) are tuned with variable shunt capacitors and 50 Ω microstrip lines on the evaluation board. After their tuning is performed, source and load second-harmonic impedances (Z_{S2}, Z_{L2}) are determined so that maximum power-added efficiency (PAE) is achieved. By varying the length of the quarter-wavelength shorted stubs

Manuscript received March 2, 1995; revised July 10, 1995.

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IEEE Log Number 9415458.

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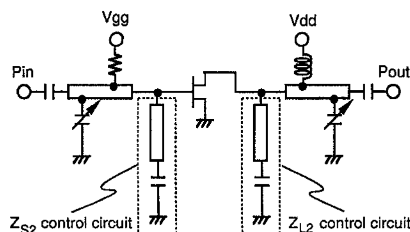


Fig. 1. Circuit diagram of the newly developed power amplifier. Z_{S1} and Z_{L1} are tuned with variable shunt capacitors and 50 Ω microstrip lines. Z_{S2} and Z_{L2} are controlled with approximate quarter-wavelength shorted stubs.

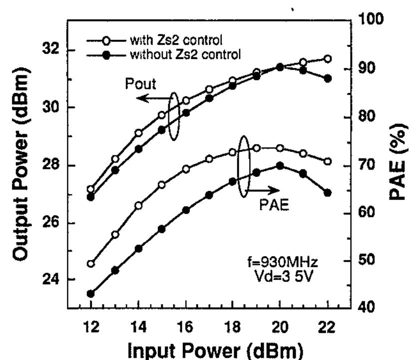


Fig. 2. Measured P_{out} and PAE of the FET at $V_d = 3.5$ V and $f = 930$ MHz under maximum PAE matching conditions. An excellent PAE of 74% with $P_{\text{out}} = 31.4$ dBm at $P_{\text{in}} = 20$ dBm is achieved under the condition of optimized Z_{S2}.

which are connected to the gate and drain electrodes on the board, Z_{S2} and Z_{L2} change around the short-circuit point along the rim of the Smith chart without affecting the values of Z_{S1} and Z_{L1}.

Power characteristics, output power (P_{out}), and power-added efficiency (PAE) under the maximum PAE matching condition are shown in Fig. 2. Measurement was carried out at a supply voltage of 3.5 V and a frequency of 930 MHz. The drain bias current was set to be 100 mA (3% of I_{dss}). Under the condition of optimized Z_{S2}, an excellent PAE of 74% with a P_{out} of 31.4 dBm and an associated gain of 11.4 dB is achieved at an input power (P_{in}) of 20 dBm. A high PAE over 70% is attained over a wide input power range of 17–22 dBm. The measured values of Z_{S1}, Z_{S2}, Z_{L1}, and Z_{L2} for the maximum PAE were; $Z_{S1} = 3.3 + j10.8$ Ω, $Z_{S2} = 1.2 + j11.7$ Ω, $Z_{L1} = 8.6 + j1.2$ Ω, and $Z_{L2} = 1.2 + j14.5$ Ω. When the Z_{S2} control circuit was removed, Z_{S2} changed to $17 + j160$ Ω without affecting Z_{S1}. In such a case, maximum PAE is limited to 70%, even if matching conditions have been tuned again at the same output power of 31.4 dBm. As a result, PAE is improved by more than 4% at around the saturation output power, and by more than 8% over a lower input power range of 13–16 dBm, by optimally controlling Z_{S2}.

Relationship between phase angle of Z_{S2} (phase(Z_{S2})) and output performance was examined. By varying the length of the quarter-wavelength shorted stub connected to the gate terminal, Z_{S2} changes around the short-circuit point along the rim of the Smith chart. Fig. 3 shows the relationship between phase (Z_{S2}) and output performance, where the values of Z_{S1}, Z_{L1}, and Z_{L2} are fixed at the above mentioned

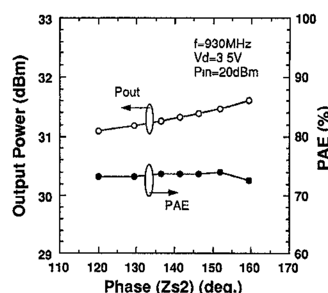


Fig. 3. Relationship between phase (Z_{S2}) and power performance of the FET.

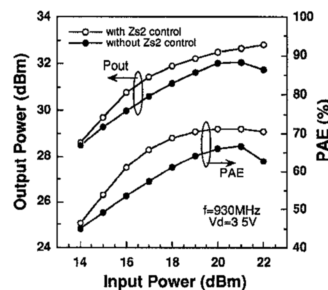


Fig. 4. Measured P_{out} and PAE of the FET under maximum P_{out} matching conditions. An increased P_{out} of 32.8 dBm at $P_{\text{in}} = 22$ dBm with a PAE of 71% is realized under the condition of controlled Z_{S2}.

conditions. The best PAE of 74% with a P_{out} of 31.4 dBm is achieved at a phase (Z_{S2}) of 152°, which corresponds to $Z_{S2} = 1.2 + j11.7$ Ω.

The FET was then evaluated under a matching condition for maximum output power ($P_{\max}$) at $V_d = 3.5$ V and $f = 930$ MHz. In order to increase output power, Z_{L1} was shifted to lower impedance ($6.0 + j0.8$ Ω) than that for maximum PAE ($8.6 + j1.2$ Ω). As shown in Fig. 4, an increased $P_{\max}$ of 32.8 dBm at $P_{\text{in}} = 22$ dBm with a high PAE of 71% and an associated gain of 10.8 dB is achieved under the condition of controlled Z_{S2}. On the other hand, $P_{\max}$ without Z_{S2} control is limited to 32 dBm at $P_{\text{in}} = 21$ dBm with a PAE of 67%. The FET with Z_{S2} control thus shows great improvement of maximum output power and PAE by 0.8 dB and 4%, respectively.

Harmonic balance simulation was performed on MDS (Commercial CAD by Hewlett Packard). Simulated P_{out} and PAE of the FET at $V_d = 3.5$ V and $f = 930$ MHz are shown in Fig. 5. By optimally controlling Z_{S2}, PAE of the FET is improved by 5% at $P_{\text{in}} = 20$ dBm. These results which agree with the measured data confirm the advantage of the Z_{S2} control technology for obtaining high efficiency amplifiers.

Gate voltage/current waveforms were analyzed by MDS. Fig. 6 shows simulated gate voltage/current waveforms at $P_{\text{in}} = 20$ dBm under two conditions (with Z_{S2} control (a), and without Z_{S2} control (b)). The gate voltage waveform with Z_{S2} control (a) is close to a square wave, in comparison with that without Z_{S2} control (b). For large-signal operation, a sinusoidal wave voltage wave inputted into the gate is transformed to a quasisquare wave, by optimally terminating Z_{S2}. This quasisquare gate voltage contributes to the reduction of the voltage/current switching time at the drain. This reduces power

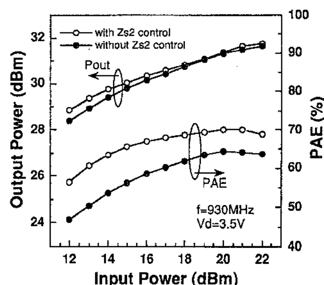
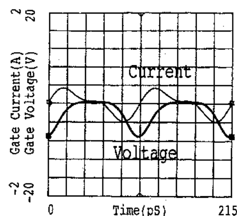
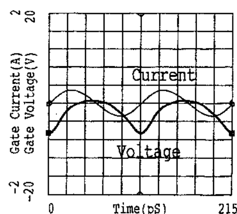


Fig. 5. Simulated P_{out} and PAE as a function of P_{in}. PAE is improved by 5% at $P_{\text{in}} = 20$ dBm by optimizing Z_{S2}.



(a)



(b)

Fig. 6. Simulated Gate voltage/current waveforms at $P_{\text{in}} = 20$ dBm under two conditions, (a) with Z_{S2} control and (b) without Z_{S2} control. The gate voltage waveform with Z_{S2} control (a) is close to a square wave.

dissipation which occurs when the drain voltage and current exist simultaneously, and results in significant improvement of PAE. In addition, the quasisquare gate voltage with a wide flat portion (at $V_g \approx 0$ V) provides a large drain current swing which is important to deliver an increased output power under limited voltage conditions.

In this simulation, the drain voltage waveform with Z_{S2} control shows a peak value of 12 V, while that without Z_{S2} control has a peak value of as low as 9 V. This indicates the new amplifier requires higher breakdown voltage (BV_{gd}).

B. Two-Stage Power Module

A two-stage GaAs power module for analog cellular phones was demonstrated. Fig. 7 shows a photograph of the power module. Two kinds of GaAs MESFET's (200 mW-FET for 1st-stage, 1.5 W-FET for 2nd-stage) with total gate width of 2 mm and 12 mm were used. The 1st-stage FET was plastic-molded in a surface mount type package. The 2nd-stage FET was assembled in a metal-based package, the bottom of which was soldered to the heat sink in order to decrease the thermal resistance. A semi-flexible printed board made of PPO (Poly-Phenylene-Oxide) with high εr (10.5) and low $\tan\delta$ (0.003) was used. The volume of the power module is 0.4 cc, which is only half of that of a conventional one [14]. The optimum tuning of Z_{S2} is only provided with the final-stage FET, on which the efficiency mainly depends. The load second-harmonic impedance (Z_{L2}) is also optimized in the output matching circuit in order to achieve both high PAE and low second-harmonic level.

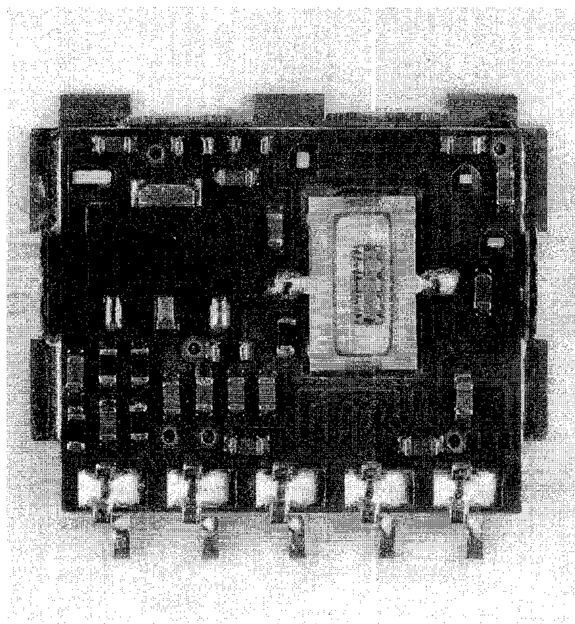


Fig. 7. Photograph of a two-stage GaAs power module, the volume of which is as small as 0.4 cc.

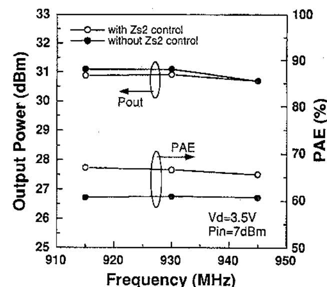


Fig. 8. Measured P_{out} and PAE of the power module. A high PAE of 66% with $P_{\text{out}} = 31$ dBm at $V_d = 3.5$ V is achieved over a frequency range of 915–945 MHz.

Fig. 8 shows measured P_{out} and PAE characteristics of the power module. A high PAE of 66% with a P_{out} of 31 dBm at $P_{\text{in}} = 7$ dBm is achieved over a frequency range of 915–945 MHz under the low supply voltage of 3.5 V. By optimally controlling Z_{S2}, PAE is improved by 6% with the same output power of 31 dBm. Supply voltage dependence of the power module was investigated. A high PAE of 66% is maintained over a supply voltage range of 2.8–3.5 V [12].

III. Linear Amplifier

A. Single-Stage Amplifier

A power amplifier employed in digital cellular systems is required to operate with low distortion. This is accomplished by backing off the output power from the saturation so as

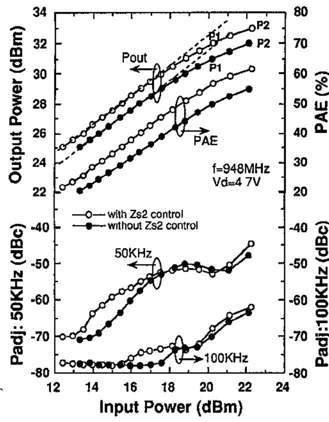


Fig. 9. Measured P_{out}, PAE and P_{adj} of the FET at $V_d = 4.7$ V and $f = 948$ MHz under the matching conditions for obtaining maximum P_{out} at 1 dB compression point (P-1dB).

to restrict the range of signal envelope variations. A GaAs MESFET with 30 mm gate-width (W_g) was fabricated by the ion-implantation technology [15]. The fabrication process of this FET was basically the same as that for saturation amplifiers mentioned in Section II. The device dimensions of L_{gs}, L_g, and L_{gd} were selected to be 1.0, 1.0, and 2.0 μm, respectively, in order to realize low distortion properties at a supply voltage of 4.7 V. The FET ($W_g = 30$ mm) had a saturation drain current (I_{dss}) of 5.0 A, and a pinch-off voltage of -2.5 V. This FET was assembled in a metal-based package.

The distortion properties of the FET ($W_g = 30$ mm) were measured on the evaluation board, the circuit diagram of which is shown in Fig. 1. Z_{S1} and Z_{L1} were tuned with variable shunt capacitors and 50 Ω microstrip lines. Z_{S2} and Z_{L2} were controlled by varying the length of the quarter-wavelength shorted stubs. An input signal was π/4-shift DQPSK modulation signal, and measurement was performed under the personal digital cellular (PDC) standard of Japanese digital cellular system. The calculation of adjacent channel leakage power (P_{adj}) is described in the Appendix.

Power characteristics, P_{out}, PAE and P_{adj} under a matching condition for obtaining maximum output power at 1 dB compression point ($P_{-1\text{dB}}$) are shown in Fig. 9. $P1$ and $P2$ denote $P_{-1\text{dB}}$ and $P_{-2\text{dB}}$ in this figure. Measurement was carried out at $V_d = 4.7$ V and $f = 948$ MHz. The drain bias current was set to be 350 mA (7% of I_{dss}). $P_{-1\text{dB}}$ with Z_{S2} control is as high as 32 dBm with a PAE of 56.5%. On the other hand, $P_{-1\text{dB}}$ without Z_{S2} control is limited to be 31 dBm with a PAE of 50%. $P_{-1\text{dB}}$ is increased by 1 dB with improvement of PAE by 6.5%. By using the Z_{S2} control technology, higher output power with improved PAE is realized not only in saturated region but also in linear region of amplification.

In addition, adjacent channel leakage power (P_{adj}) with Z_{S2} control is almost the same as that without Z_{S2} control over an input power range of 18–22 dBm. The reason why P_{adj} with Z_{S2} control seems slightly greater in the linear region (input power of less than 18 dBm) is mainly because with Z_{S2} control the FET provides higher output power by almost 1 dB at the same input power.

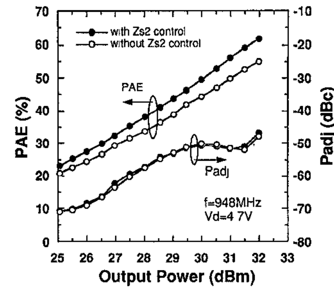


Fig. 10. Measured PAE and P_{adj} of the FET as a function of P_{out} under maximum PAE matching conditions with P_{adj} below -50 dBc at $P_{\text{out}} = 31.5$ dBm.

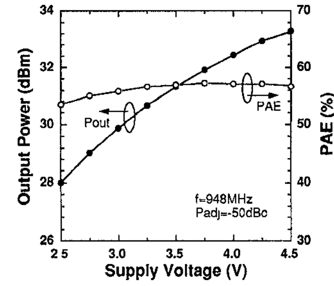


Fig. 11. Relationship between supply voltage and power performance with P_{adj} at 50 kHz offset point below -50 dBc. An excellent PAE of 57% with a P_{out} of 31.3 dBm was achieved at $V_d = 3.5$ V.

The FET was then evaluated under maximum PAE matching condition with P_{adj} (50 kHz offset point) below -50 dBc at $P_{\text{out}} = 31.5$ dBm. PAE and P_{adj} as a function of P_{out} are shown in Fig. 10. Under the condition of optimized Z_{S2}, an excellent PAE of 59% with an associated gain of 10.8 dB is achieved at a P_{out} of 31.5 dBm. In case without Z_{S2} control, PAE is limited to 52.5% with an associated gain of 10.4 dB. By optimally controlling Z_{S2}, PAE is improved by 6.5% at $P_{\text{out}} = 31.5$ dBm, while P_{adj} characteristics under the both conditions agree very well over a wide output power range. A decrease in the improvement of PAE together with a decrease in the output power suggests that a voltage wave at the gate terminal could not be transformed to a quasisquare wave for low output power operation although Z_{S2} was optimally terminated.

Relationship between supply voltage and power performance with P_{adj} at 50 KHz offset point below -50 dBc was evaluated under the condition of optimized Z_{S2}. The matching conditions were fixed to obtain the best performance at $V_d = 3.5$ V. As shown in Fig. 11, an excellent PAE of 57% with a P_{out} of 31.3 dBm is achieved at $V_d = 3.5$ V. 30 dBm (1 W) output power with a PAE of 56% is also realized at the low supply voltage of 3.0 V.

B. Two-Stage Power Module

A two-stage GaAs power module for digital cellular phones was also demonstrated. The specification of output power of PDC handsets are 28 dBm with P_{adj} of less than -45 dBc and less than -60 dBc at 50 kHz and 100 kHz offset point from center frequency, respectively. The power module should

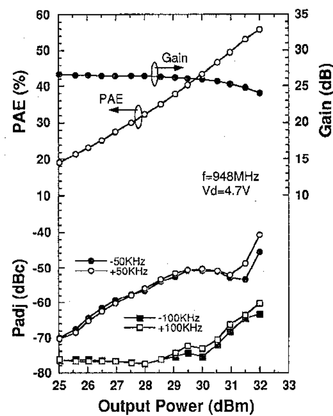


Fig. 12. Input-output properties of the power module at $V_d = 4.7$ V and $f = 948$ MHz. A high PAE of 50% with $P_{\text{out}} = 31$ dBm and $P_{\text{adj}} = -52$ dBc is achieved.

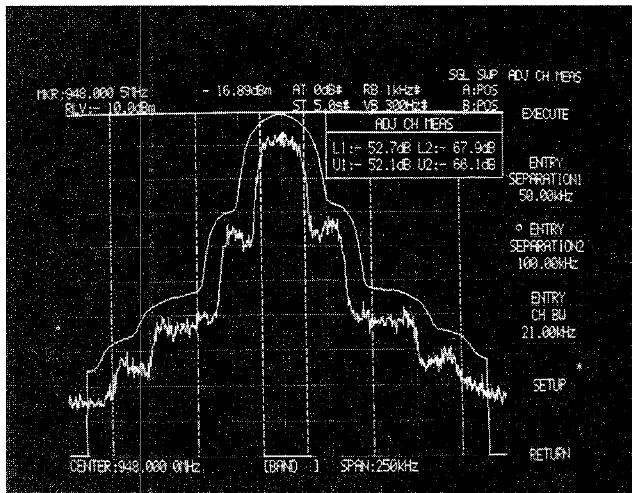


Fig. 13. The output signal spectrum of the power module at $P_{\text{out}} = 31$ dBm and $f = 948$ MHz.

achieve P_{out} of 31 dBm with P_{adj} of less than -50 dBc and less than -65 dBc at 50 kHz and 100 kHz offset point respectively, with the loss and the degradation between the power module and the antenna taken into account. The size and configuration of this power module are basically the same as that for analog cellular phones mentioned above, in which two kinds of GaAs MESFET's with total gate-width of 6 mm and 30 mm are used. The 1st-stage FET with 6 mm gate-width delivers a P_{out} of 22 dBm at $V_d = 4.7$ V and $f = 948$ MHz with P_{adj} of less than -55 dBc at 50 kHz offset point.

Fig. 12 shows input-output properties with PAE and P_{adj} at $V_d = 4.7$ V and $f = 948$ MHz. Idle currents of 1st and 2nd stage FET's were set to be 80 mA and 350 mA, respectively. A high PAE of 50% with a P_{adj} of -52 dBc and an associated gain of 25 dB is achieved at $P_{\text{out}} = 31$ dBm. This PA module exhibits $P{-}1$ dB and $P{-}2$ dB of 30.5 dBm and 31.6 dBm, respectively. Fig. 13 shows the output signal spectrum at $P_{\text{out}} = 31$ dBm and $f = 948$ MHz. The upper curve in this figure is the integrated power envelope. $L1$, $U1$, $L2$, and $U2$ denote P_{adj} at -50 kHz, $+50$ kHz, -100 kHz and $+100$ kHz offset point from the center frequency, respectively.

The carrier frequency range of the PDC system is from 940 MHz to 956 MHz. In this frequency range, this power module achieves a high PAE of 50% with $P_{\text{out}} = 31$ dBm and P_{adj} of less than -50 dBc at $V_d = 4.7$ V. This value of PAE is one of the highest ever reported.

TABLE I
POWER PERFORMANCE OF SINGLE-STAGE AMPLIFIERS AND TWO-STAGE POWER MODULES

	Type	Vd (V)	Pout (dBm)	PAE (%)
Saturated Amplifier	Single-Stage	3.5	31.4	74
	Two-Stage Module	3.5	31	66
Linear Amplifier	Single-Stage	4.7	31.5	59
		3.0	31	56
	Two-Stage Module	4.7	31	50

Note -Saturated Amplifier was measured at 930MHz.
-Linear Amplifier was measured with keeping Padj of bellow -50dBc at 50KHz offset point from 948MHz

IV. CONCLUSION

The effects of tuning source second-harmonic impedance (Z_{S2}) on output power and efficiency of the GaAs MESFET's have been studied at 900 MHz band. By optimally terminating source and load second-harmonic impedances (Z_{S2}, Z_{L2}) as well as the fundamental impedances, a record high 74% PAE with a P_{out} of 31.4 dBm (1.4 W) at 930 MHz has been achieved as a single-stage saturated amplifier using an ion-implanted GaAs MESFET ($W_g = 12$ mm) under the low supply voltage of 3.5 V. When tuned for maximum output power, 32.8 dBm (1.9 W) output power with a PAE of 71% has been realized. As a result of harmonic balance simulation, it has been confirmed that a sinusoidal voltage wave inputted into the gate can be transformed to a quasisquare wave for large-signal operation by optimally terminating Z_{S2}.

This technology has been also useful to achieve high efficiency linear amplifiers. An excellent PAE of 59% with 31.5 dBm output power and P_{adj} below -50 dBc at 50 KHz offset point has been realized as a single-stage linear amplifier using the GaAs MESFET (W_g =30 mm) at $V_d = 4.7$ V and $f = 948$ MHz.

Saturated and linear power modules (two-stage amplifier) have been demonstrated for analog and digital cellular applications respectively, the volume of which is as small as 0.4 cc. The saturated power module has delivered 66% PAE with a P_{out} of 31 dBm (1.25 W) over a frequency range of 915–945 MHz at $V_d = 3.5$ V. The linear one has exhibited 50% PAE with a P_{out} of 31 dBm and P_{adj} of less than -50 dBc over a frequency range of 940–956 MHz at $V_d = 4.7$ V. The excellent performance strongly indicates the advantage of the new technology for high power and high efficiency amplifiers. The power performance of single-stage amplifiers and two-stage power modules are summarized in Table I.

APPENDIX

P_{adj} was calculated by the spectrum analyzer (Anritsu MS2602A) as follows

$$P_{\mathrm{adj}} = 10\log\left(\int_{Af-B/2}^{Af+B/2} p(f)\,df / P_{\mathrm{total}}\right)$$

Here,

f : frequency

Af : center frequency(Cf) +/−50 kHz or +/−100 kHz

B : band width of 21 kHz

$p(f)$: measured power at each frequency

P_{total} : total power of the spectrum

P_{total} is expressed as,

$$P_{\mathrm{total}} = \int_{-\infty}^{+\infty} p(f)\,df \approx \int_{\mathrm{Cf-SB/2}}^{\mathrm{Cf+SB/2}} p(f)\,df.$$

Here,

Cf: center frequency of the signal.

SB: band width of 250 kHz (full span of the spectrum analyzer in the measurement).

ACKNOWLEDGMENT

The authors wish to thank M. Inada, K. Inoue, and A. Tamura for their encouragement. The authors are also grateful to M. Miura for his earnest technical assistance.

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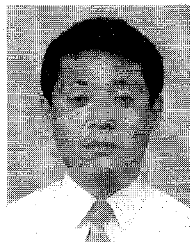

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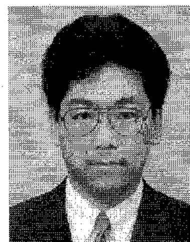

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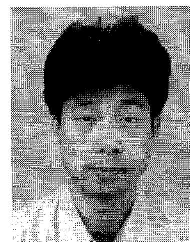

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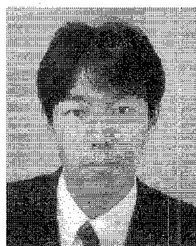

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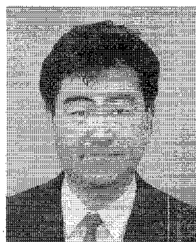

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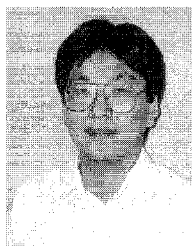

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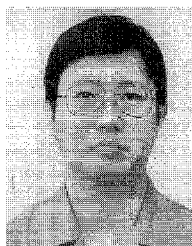

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